



**University
of Victoria**

Graduate Studies

Notice of the Final Oral Examination
for the Degree of Master of Applied Science

of

SALMAN KHAN

BS (Sir Syed University of Engineering and Technology, 2010)

“VHDL Implementation and Performance Analysis of two Division
Algorithms”

Department of Electrical and Computer Engineering

Wednesday, July 22, 2015

10:30 A.M.

Engineering Office Wing

Room 430

Supervisory Committee:

Dr. Fayez Gebali, Department of Electrical and Computer Engineering,
University of Victoria (Co-Supervisor)

Dr. Atef Ibrahim, Department of Electrical and Computer Engineering, UVic (Co-Supervisor)

External Examiner:

Dr. Yvonne Coady, Department of Computer Science, UVic

Chair of Oral Examination:

Dr. Steve Perlman, Department of Biology, UVic

Abstract

Division is one of the most fundamental arithmetic operation and is used extensively in engineering, scientific, mathematical and cryptographic applications. The implementation of arithmetic operation such as division, is complex and expensive in hardware. Unlike addition and subtraction, division requires several iterative computational steps on given operands to produce the result. Division, in the past has often been perceived as an infrequently used operation and received not as much attention but it is one of the most difficult operation in computer arithmetic. The techniques of implementation in hardware of such an iterative computation impacts the speed, the area and power of the digital circuit. For this reason, we consider two division algorithms based on their step size in shift. Algorithm 1 operates on fixed shift step size and have fixed number of iteration while the Algorithms 2 operates on variable shift step size and requires considerably lesser number of iterations. In this thesis, the technique is provided to save power and speed up the overall computation. It also looks at different design goal strategies and presents a comparative study to asses how each of the two design perform.